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Performance Analysis and Hardware Implementation of Digital Circuit Design Using Reversible Logic

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Abstract: *Reversible logic approach of designing is gaining its attention by researchers due to its characteristics of dissipating less power. Reversible logic technology do not erase information hence no heat dissipation. In this paper,various reversible combinational and sequential circuits are proposed such as Multifunction Generator, 4-bit Full/Subtractor, 4-bit Fast carry chain adder and 4-bit asynchronous counter by the proposed reversible T-flip flop.The proposed circuits hasbeen designed for low power, less area and high speed based on the designs, also multifunction generator with zero garbage output can be seen. The power, speed and area parameters for the circuit have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are more efficient. The designs presented in this paper were simulated using Xilinx 14.2 software.*
Key Terms: *Low Power, Less Area,High Speed, Reversible design.*

I. Introduction

Reversible logic is widely used in low power VLSI applications. Landauer showed that combinational logic circuits dissipate heat of the order of KT In2 joules [1] for every bit of information that is lost. As Reversible circuits are capable of back-computation andthere is no loss of information,we find reduction in dissipated power with higher speed and higher density. Any circuit is said to be reversible if there exists a unique output for each input i.e., number of inputs must be equal to number of outputs, making it logically reversible. And an operation is said to be physically reversible if it converts no energy to heat and produces noentropy. A logic circuit is said to be reversible, if there is one-to-one correspondence between inputs and outputs with no loss of information. This permits the system to run backwards and while doing so, any intermediate design stage can be comprehensively examined. The fan-out of reversible logic circuit has to be one and only one.

In any reversible design garbage outputs and number of reversible gates are two of the importantdesign parameters which must be as minimum as possible. To evidence this multifunction generator[2]which is able to change its function in an expected, controllable and required way, is been proposed with no zero garbage outputs, less number of reversible gates using reversible logic. Secondly in any digital system, adder and subtractorblock, flip-flop or

Counterare the most essential one. And an integration of these blocks becomes essential sometimes thus; full adder/subtractor isused in most digital systems. In the present day consequence, technology scaling is believedto be at its greater summits and further scaling leads to lots ofcomplexities. Hence, there is a need for a low power circuits with optimized area and high speeds. Reversible logic is one of the answers forthe above problem which is evolving as a performance substitute for conventional logic. Thus to substantiate, a new 4-bit reversible full adder/subtractor,4-bit fast carry chain adder[3] and 4-bit asynchronous ripple counter[4]is proposed using reversible logic that are performance efficient with respect to power, area and speed[1].

II. Reversible Logic

A Boolean logic is supposed to be reversible if, the following conditions are encountered [5]

1. Condition 1
   A reversible logic gate must have some features such as equal number of input and output signals, one to one mapping between inputs and outputs that has been entitled as " Bi-jective Conditions"
2. Condition 2
   From the total number of input combinations, half of its input combinations must have an output equal to 1, entitled as "Balance Conditions".
3. Condition 3
   By inversing output, we must be able to reproduce mapped input entitled as "Inversing Conditions".

The important design constraints for reversible logic circuits are stated below [5]

1. Reversible logic circuits do not allowmore than one fan-out.
2. Reversible logic circuits should have minimum quantum cost.
3. With minimum number of garbage outputs the design can be optimized.
4. Minimum number of constant inputs must be used for reversible logic circuits.
5. The reversible logic circuits must use a minimum gate levelsi.e. delay of the circuit.

III. Reversible Gates

There are many reversible gates such as Feynman, Double Feynman, Toffoli, TSG, Fredkin, Peres, etc.[6]. As NAND and NOR are universal gates in Boolean logic, for reversible logic, the universal gates are Feynman and Toffoli gates.

1. Feynman Gate: Feynman gate[6] is 2*2universal reversible gate represented as 'F'gate. It has been used for signal replication purposes or to getthe complement of the input signal. The block diagram of Feynman gate is shown in Figure1:

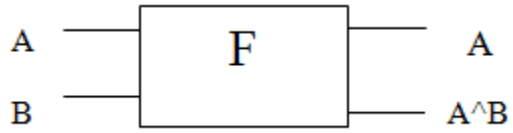

Figure 1: Feynman Gate

2 Toffoli Gate: Toffoligate[6] which is a 3*3 gate being one of the universal reversible gate. With inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C. It has been used for extracting the AND or NAND operation. The block diagram of Toffoli gate is as shown in Figure 2:

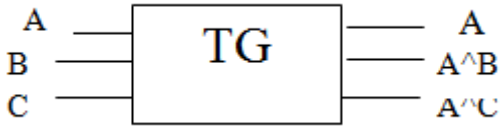

Figure 2: Toffoli Gate

3. SMT Gate: It [5] is a new 3*3reversible logic gate named after the proposed persons Singh Mishra Tiwari. SMT gate has been designed for Logical, a Boolean and Arithmetical function that acts solely as 1-bithalf adder/substrator.Its Block diagram is as shown in Figure 3:

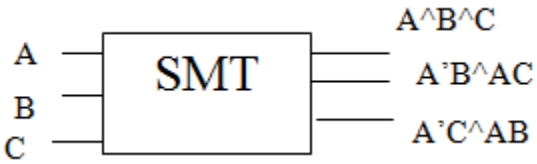

Figure 3: SMT Gate

4. COG Gate: COG (Controlled Operation Gate) gate[7] is a 3*3 reversible gate whose block diagram is shown in Figure 4. In this gate the input vector is given by Input Vector(IV) = (A, B, C) and the corresponding output vector is Output Vector (OV)= (P, Q, R) as shown in its block diagram below in Figure 4.It solely acts as 2x1 multiplexer with A being the select line.

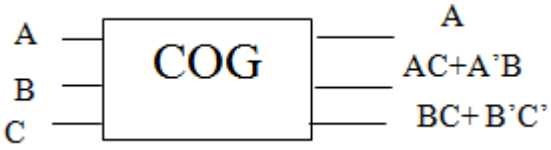

Figure 4: COG Gate.

5. NPPRG: It [8] is a new 4*4reversible gate. The NPPRG (New Parity PreservingReversible Gate) block diagramis shown in Figure 5. As the name implies NPPRG was proposed for parity preservation, however it also has multifunctioning capability.

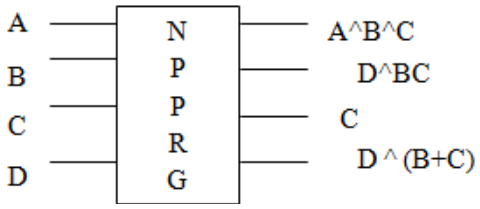

Figure. 5: NPPRG Gate

IV. Multifunction Generator

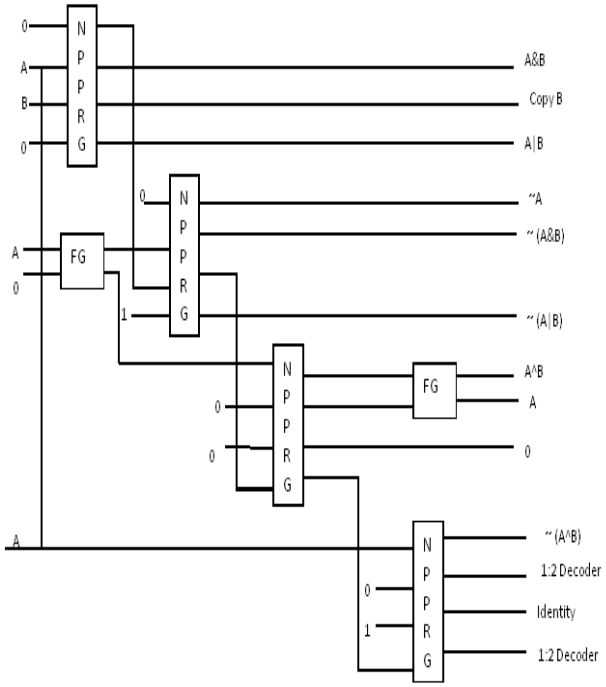

Figure 6: Multifunction Generator with zero garbage output

Implementation of multifunctional logic gates may be different.Multifunctional logic can be implemented using conventional gatesor may be implemented using new methods such as Reversible Logic. While attempting to design with reversible logic meeting two of its constraints, minimum garbage outputs as possible and minimum number of reversible gates, came up with new design meeting these constraints, than the existing design of multifunction generator. Here we attempted to design Multifunction Generator using the proposed NPPRG Reversible Gate generating 12 Functions with zero garbage outputs and minimum gates when compared to existing design[7] as shown in Figure 6. The list of functions are tabulated in the below Table 1.

Table 1: Functions Generated

Boolean Function	**Function Name**
A.B	AND
Copy B	COPY B OPERATION
A+B	OR
B’	NOT
(A.B)’	NAND
(A+B)’	NOR
A^B	XOR
Copy A	COPY A OPERATION
0	NULL
(A^B)’	XNOR
1	IDENTITY
B or B’	1:2 DECODER

V. Proposed Reversible Combinational Circuits

A.Proposed 4-Bit Reversible FullAdder/Subtractor

In digital circuits, an adder/subtractor circuit that is capable of integrating bothadding or subtracting numbers (in particular, binary) one at a time with control input becomes essential during periods. Below is a circuit Figure 7(a)that shows 1-bit full adder/subtractor using reversible SMT (Singh Mishra Tiwari) gate acting solely as half adder/subtractor along with the reversible COG gate acting as multiplexer. Using the proposed 1-bit adder/subtractor, 4-bit parallel adder/subtractor is proposed that is shown in Figure 7(b) below.

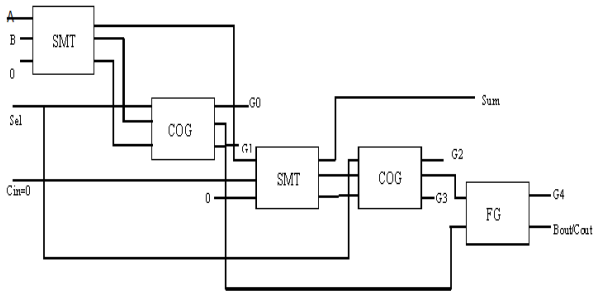

Figure. 7(a): 1-Bit Reversible Full Adder/Subtractor

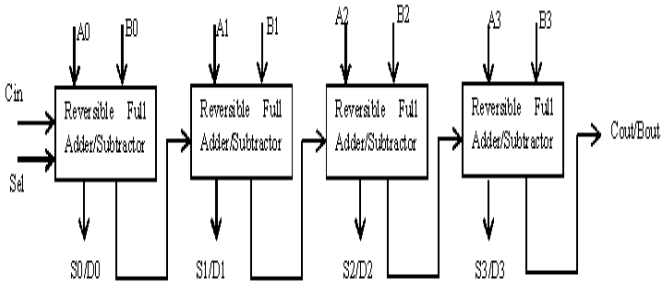

Figure. 7(b): 4-Bit Reversible Parallel Adder/Subtractor

B.Proposed 4-Bit Reversible Fast Carry Chain Adder

Carry values at each position can be more easily determined than in ripple carry method by reformulating the carry look head equations as below[3]

$S_i = P_i \wedge C_i$ (i)

$C_{i+1} = G_i + P_i C_i$ (ii)

If propagating signal P_i driving the multiplexer (MUX) is 0 then carry is generated or eliminated thus allowing to select either of the inputs of MUX to drive the carry out without actually waiting for carry in and if propagating signal P_i driving the MUX is then carry out generated will be same as carry in.

In order to enhance the speed of the fast carry chain adder as in the conventional approach, here we try to propose 4- bit reversible fast carry chain adder that enhance the speed further more using reversible approach as shown in Figure 7(d) below.1-bit fast carry chain adder is shown in Figure 7(c)

It uses 2 COG gate and 1 FG gate.

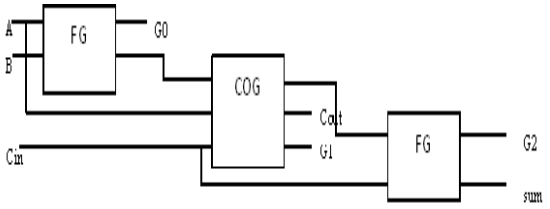

Figure. 7(c): 1-Bit Reversible Full Adder/Subtractor

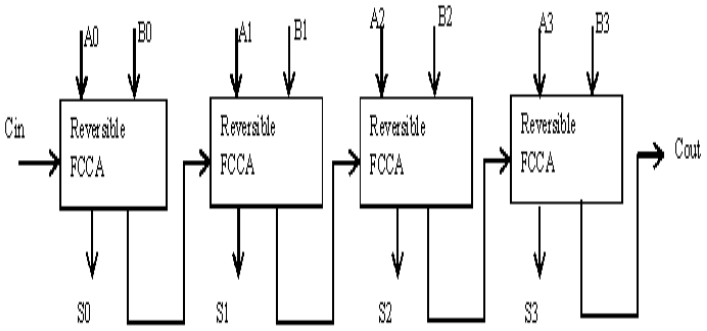

Figure 7(d): 4-bit Reversible Fast carry chain adder

VI. Proposed Reversible Sequential Circuits[9]

A. Proposed 1-Bit Reversible T-Flipflop

Initially D-Flip-flop is designed using 3 reversible SR latches with clear input signal. Flip-flop reacts during the negative edge of the clock input signal thus producing reversible negative edge triggered D-Flip-flop[8] as shown in Figure 8(a). This particular D-flip-flop is used in proposing reversible T-flip-flop by connecting inverting output of D-Flip-flop back to its input again leading to negative edged T-Flipflop.The block diagram of Negative edge T-Flip-flop is as shown below in Figure 8(b):

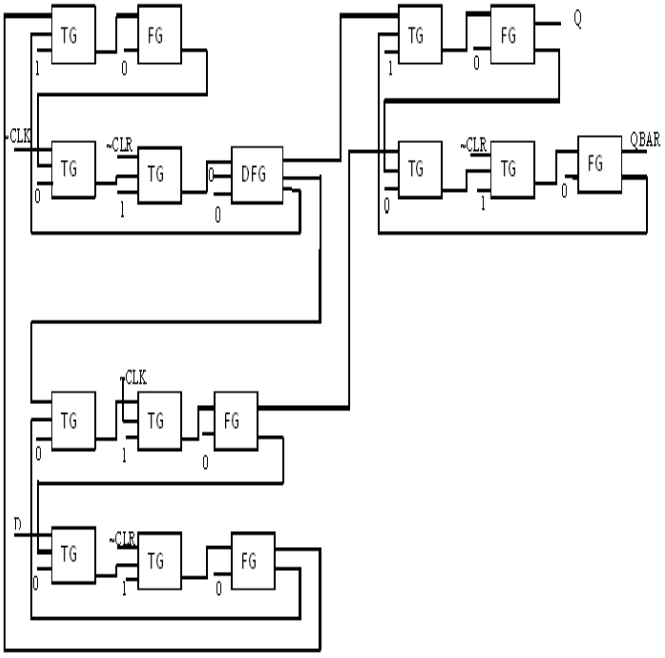

Figure 8(a): 1-bit Reversible D-flip-flop

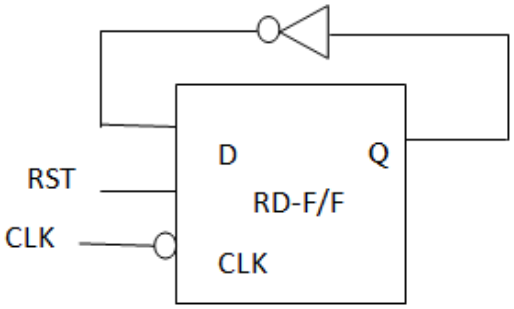

Figure 8(b): 1-bit Reversible T-flip-flop

B. Proposed 4-Bit Reversible Asynchronous Ripple Counter[8]

The asynchronous ripple counter here is constructed by T-flip flop by connecting q output of each T flip flop to the clock input of the other T-flip-flop. Also theT-flip flop is constructed by connecting inverted q output to the d input. Thus the counter increments on negative edges. The Table 2 shows the truth table of the asynchronous ripple counter.

Table 2: Truth table for Asynchronous Ripple Counter

Clk	Q1	Q2	Q3	Q4
1	0	0	0	0
0	0	0	0	1
0	0	0	1	0
0	0	0	1	1
0	0	1	0	0
0	0	1	0	1
0	0	1	1	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1

The Figure 8(c) below shows the 4-bit reversible Asynchronous ripple counter designed using TG,FG & DFG reversible gates, proposed using reversible approach to enhance the area and speed of the proposed system.

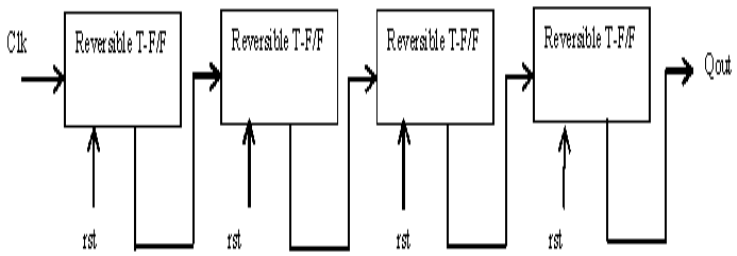

Figure 8(c): 4-bit reversible Asynchronous Ripple Counter

VII. Results

1.Proposed Design of Multifunction Generator

	Gate Count	**No. of Garbage Outputs**	**No. of Functions**
Existing Design[7]	8	2	8
Proposed Design	6	0	12

2. Reversible Combinational circuits

2.1. 4-bit reversible Parallel Adder/Subtractor with control signal

Parameter	**Irreversible logic**	**Reversible logic with control**
Power	1595.77mW	1578.10mW
Area (No. of LUTs)	7	6

2.2. 4-bit reversible Fast carry chain adder

Parameter	**Irreversible logic**	**Reversible logic**
Speed	4.674nsec	4.530nsec
Area (No. of LUTs)	7	6
Power	1589.86W	1589.86mW

3.Reversible Sequential Circuit

A. 4-bit Reversible Asynchronous Ripple Counter

Parameter	Irreversible logic	Reversible logic
Speed(Max Clock Frequency)	78.85MHz	114.10MHz
Area (No. of LUTs)	16	12

VIII. Conclusion

In this paper, it can be seen that the performance of digital circuits can be enhanced using reversible gates.One of the majorconstraints in reversible logic is to minimize the number of reversible gates used and garbage outputsproduced thus, realising multifunction generator with less gate count, zero garbage outputs. Furthermore, 4-bit reversible Parallel adder/subtractor, 4-bit Fast carry chain adder and 4-bit reversible asynchronous ripple counter were designed. Lastly all these were simulated in Xilinx 14.2 tool and respective results validate prior inferences. Thus, all the designs implemented were compared withtheir irreversible counterparts, and Power, area, speed parameters for the reversible designs were observed to have improved significantly.

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